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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,226	06/12/2001	Roger May	015114-053300US	7601

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/881,226	MAY ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 46-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 46-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

SCE

STEPHEN C. ELMORE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 5/6/2005.

Drawings

1. The drawings are objected to because Figure 7 contains unclear context printed with graphite in the embedded processor strip, which is unreadable. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-4, 7-10, 46-51 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winegarden et al. (US PAT. 6,467,009 hereinafter Winegarden) in view of Sugita (US PAT. 5,276,842).

Regarding claim 1, Winegarden discloses a configurable system including an embedded processor portion coupled to a programmable logic (210, figure 2) via an internal system bus, wherein the embedded processor portion comprising a processor (210, figure 2) coupled with a memory block (255, figure 2), wherein the bus includes an arbiter (315, figure 3) connected to the memory (figure 2, col. 4 line 30 through col. 5 line 43). Winegarden differs from the claimed

invention in not specifically teaching the memory block comprising a memory having a first port and the second port, wherein the arbiter arbitrates access to the memory by the first port and the second port. However, Sugita teaches to utilize a memory block including a dual port memory (50, figure 10) for improving the throughput of the system, wherein the memory block also comprises an arbiter (51, figure 10) coupled to the a first port, i.e., A port, and a second port, i.e., B port, for accessing to the memory by the first ports and the second port, for avoiding contention between write access and read access (col. 7 line 27 through col. 8 line 39 and col.20 lines 16-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Winegardan in having memory block comprising a memory having a first port and the second port, wherein the arbiter arbitrates access to the memory by the first port and the second port, as per teaching of Sugita, because it improves the throughput of the system (col. 5 lines 8-9).

Regarding claim 2, Sugita discloses the memory being a dual port SRAM (figure 5 and col. 2 line 52).

Regarding claim 3, Winegardan discloses the programmable logic portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic function (figure 10 and col. 9 line 55 through col. 10 line 54).

Regarding claim 4, Winegardan discloses the programmable logic portion comprising a plurality of horizontal and vertical interconnect lines programmably coupled to the plurality of logic elements (figure 10).

Regarding claim 7, Winegardan discloses a programmable logic integrated circuit (210, figure 2) comprising a programmable logic portion having a plurality of logic elements,

programmable configurable to implement user defined combinational or registered logic functions (figure 10 and col. 9 line 55 through col. 10 line 54), and an embedded processor portion and comprising a processor (220, figure 2) and a memory block (255, figure 2) coupled to the processor and comprising a plurality of memory cells for storing data. Winegarden differs from the claimed invention in not specifically teaching the memory block comprising a first plurality of memory cell for storing data, a second plurality of memory cells for storing data, a first port coupled to the first and second plurality of memory cells, a second port coupled to the first and second plurality of memory cells, and a arbiter coupled to the first port and the second port, memory cells, the arbiter prevents the first port from accessing the plurality of memory cells, and allow the first port to access the second plurality of memory cells when the second port is accessing the subset of the first plurality of memory cells. However, Sugita teaches to utilize a memory block including a dual port memory (50, figure 10) for improving the throughput of the system, wherein the memory block also comprises an arbiter (51, figure 10) coupled to the a first port, i.e., A port, and a second port, i.e., B port, for accessing to the memory by the first ports and the second port, for avoiding contention between write access and read access (col. 7 line 27 through col. 8 line 39 and col.20 lines 16-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Winegardan in having the memory block comprising a first plurality of memory cell for storing data, a second plurality of memory cells for storing data, a first port coupled to the first and second plurality of memory cells, a second port coupled to the first and second plurality of memory cells, and a arbiter coupled to the first port and the second port, memory cells, the arbiter prevents the first port from accessing the plurality of memory cells, and allow the first port to access the second plurality of

memory cells when the second port is accessing the subset of the first plurality of memory cells, as per teaching of Sugita, because it improves the throughput of the system (col. 5 lines 8-9).

Regarding claim 8, Sugita discloses the first plurality of memory cells and the second plurality of memory cells being defined by a user programmable lock register (col. 7 lines 62-68).

Regarding claim 9, Sugita discloses the first and second plurality of memory cells comprising a portion of dual-port SRAM (figure 5 and col. 2 line 52).

Regarding claim 10, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 46, Sugita teaches the arbiter allows the first port to access the first plurality of memory cells when the second port is accessing a subset of the second plurality of memory cells and the arbiter allows the first port to access the second plurality of memory cells when the second port is accessing the subset of the first plurality of memory cells (col. 7 line 27 through col. 8 line 39 and col.20 lines 16-27).

4. Claims 5-6, 11-12 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winegarden et al. (US PAT. 6,467,009 hereinafter Winegarden) in view of Sugita (US PAT. 5,276,842) as applied in claims above, and further in view of Phelan et al. (US PAT. 6,499,089 hereinafter Phelan).

Regarding claims 5-6, the combination of Winegarden and Sugita differs from the claimed invention in not specifically teaching the second port as well as the first port being configurable in width and depth. However, Phelan teaches an integrated circuit having both first

and second ports being configurable in width and depth (col. 2 lines 11-14) in order to allow different width of data to be read out from the memory based upon the requirements of different processors, thereby improving memory versatility (col. 4 lines 39-42). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Winegarden and Sugita in having the second port, as well as the first port, being configurable in width and depth, as per teaching of Phelan, in order to allow different width of data to be read out from the memory based upon the requirements of different processors, thereby improving memory versatility.

Regarding claims 11- 12, the limitations of the claims are rejected as the same reasons set forth in claims 5-6.

Regarding claim 52, the limitations of the claim are rejected as the same reasons set forth in claim 5-6.

Response to Arguments

5. Response to Arguments Applicant's arguments with respect to claims 1-12 and 46-53 have been considered but are moot in view of the new grounds of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:30 AM-6:00 PM, and alternate Monday 8:30 AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li
Patent Examiner
Art Unit 2189

STEPHEN C. ELMORE
PRIMARY EXAMINER